ABSTRACT OF THE DISCLOSURE

The present invention facilitates clock and data recovery (330,716/718) for serial data streams (317,715) by providing a mechanism that can be employed to maintain a fixed tracking capability of an interpolator based CDR circuit (300,700) at multiple data rates (e.g.,800). The present invention further provides a wide data rate range CDR circuit (300,700), yet uses an interpolator design optimized for a fixed frequency. The invention employs a rate programmable divider circuit (606,656,706) that operates over a wide range of clock and data rates (e.g.,800) to provide various phase correction step sizes (e.g.,800) at a fixed VCO clock frequency. The divider (606,656,706) and a finite state machine (FSM) (612,662,712) of the exemplary CDR circuit (600,650,700) are manually programmed based on the data rate (614,667). Alternately, the data rate may be detected from a recovered serial data stream (718) during CDR operations (on-the-fly) utilizing a frequency detection circuit (725) to automatically program the divider (706) and FSM (712) to provide CDR circuit operation at the nearest base clock rate (716).